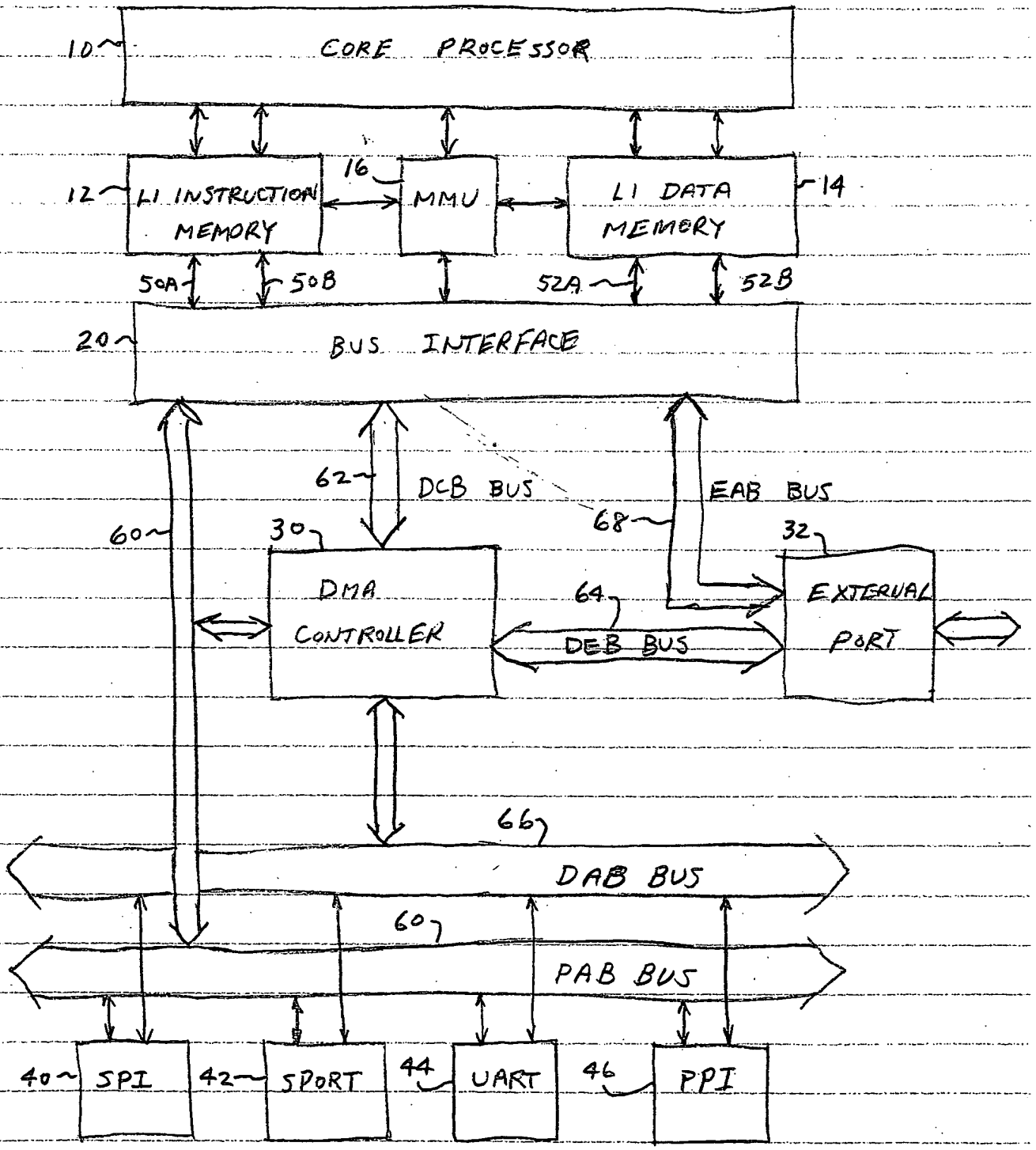
10
CORE PROCESSOR
12
L1 INSTRUCTION MEMORY
16
MMU
L1 DATA MEMORY
14
50A
50B
52A
52B
20
BUS INTERFACE
62
DCB BUS
EAB BUS
68
60
30
DMA CONTROLLER
64
DEB BUS
32
EXTERNAL PORT
66
DAB BUS
60
PAB BUS
40
SPI
42
SPORT
44
UART
46
PPI

FIG. 1

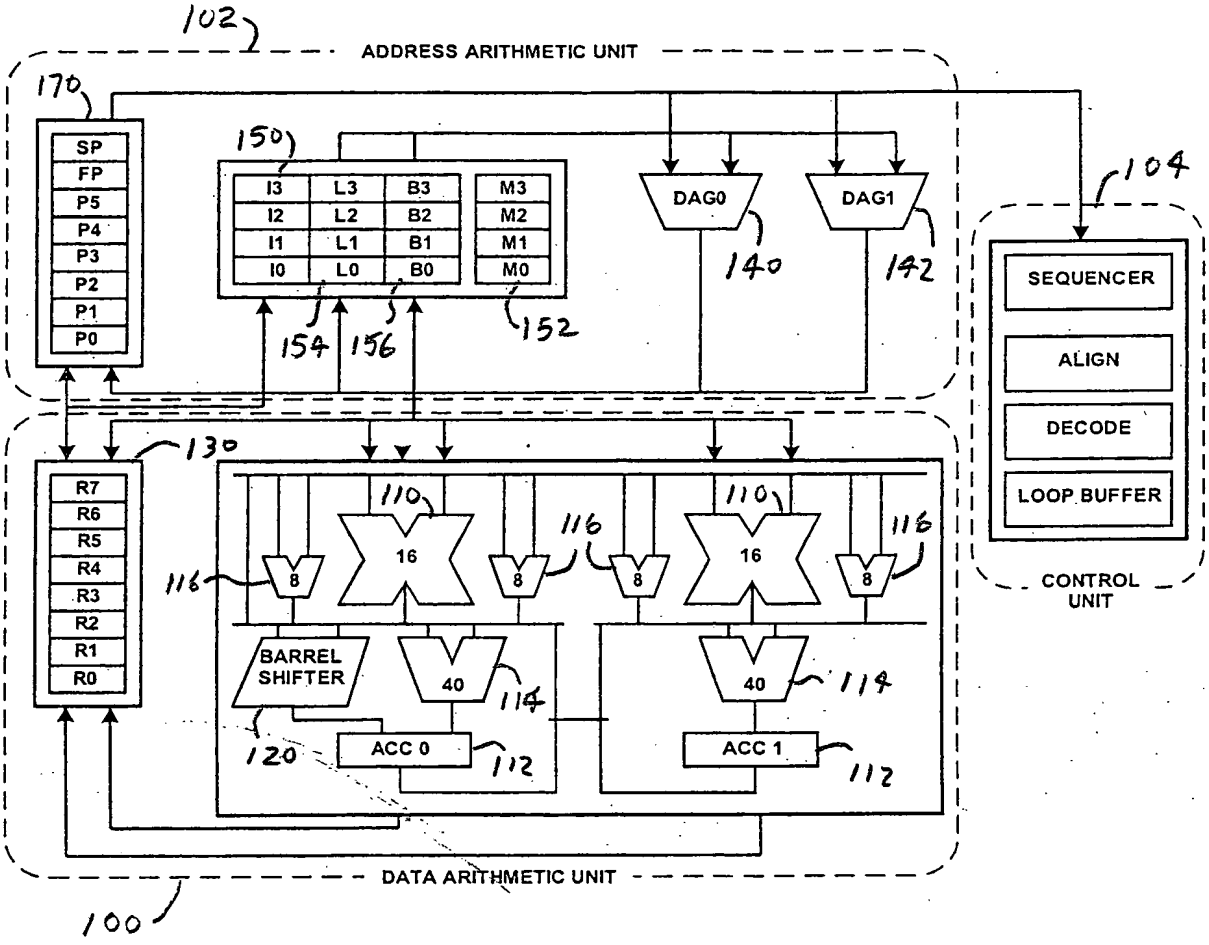
102
ADDRESS ARITHMETIC UNIT
170
SP
FP
P5
P4
P3
P2
P1
P0
150
I3
I2
I1
I0
L3
L2
L1
L0
B3
B2
B1
B0
M3
M2
M1
M0
154
156
152
DAG0
DAG1
140
142
104
SEQUENCER
ALIGN
DECODE
LOOP BUFFER
CONTROL UNIT
130
R7
R6
R5
R4
R3
R2
R1
R0
110
16
8
116
BARREL SHIFTER
40
114
120
ACC 0
ACC 1
112
DATA ARITHMETIC UNIT
100

FIG. 2

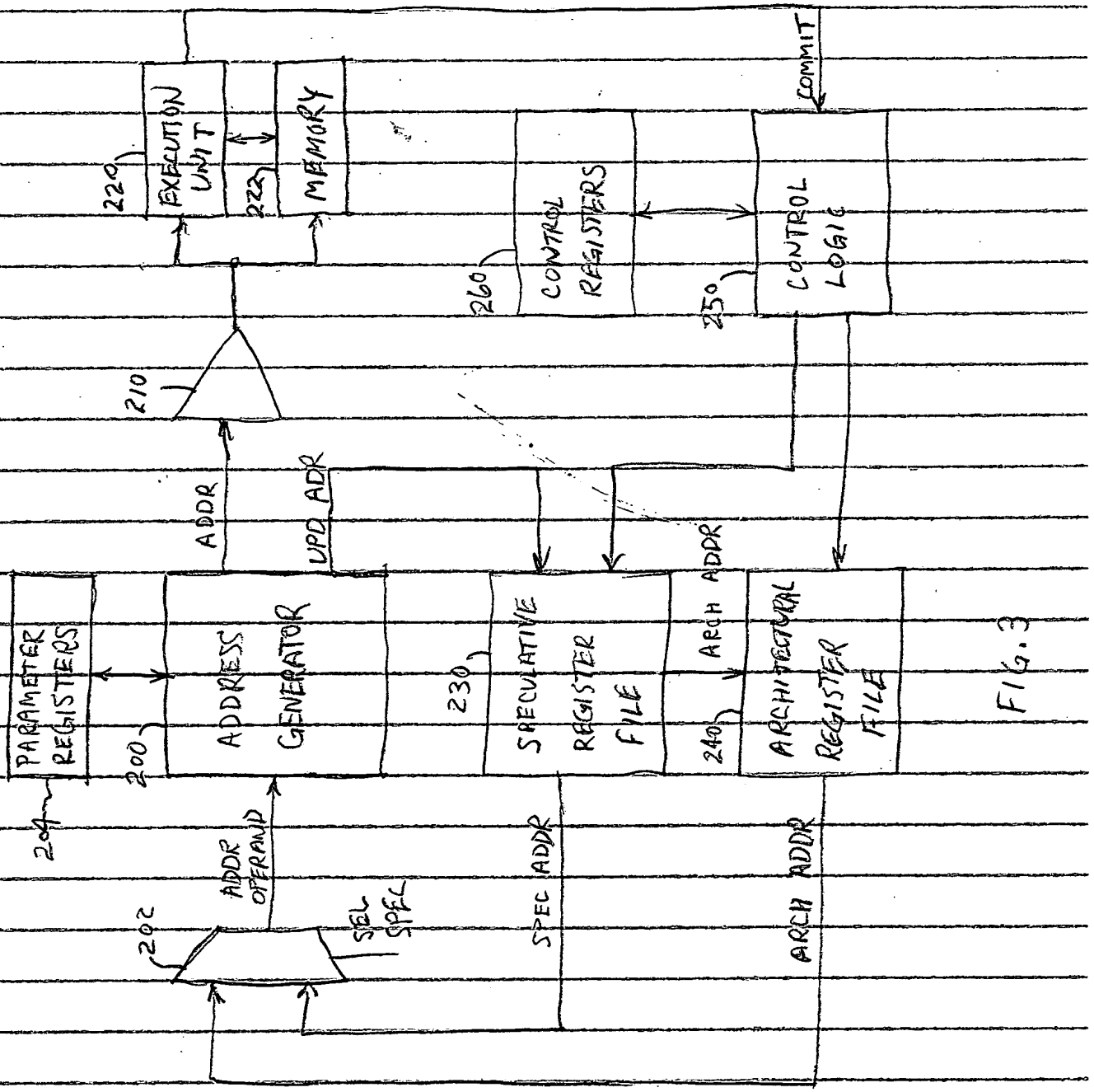
COMMIT
220
EXECUTION UNIT
222
MEMORY
260
CONTROL REGISTERS
250
CONTROL LOGIC
210
ADDR
UPD ADR
PARAMETER REGISTERS
204
200
ADDRESS GENERATOR
230
SPECULATIVE REGISTER FILE
ARCH ADDR
240
ARCHITECTURAL REGISTER FILE
ADDR OPERAND
SPEC ADDR
ARCH ADDR
202
SEL
SPEC

FIG. 3

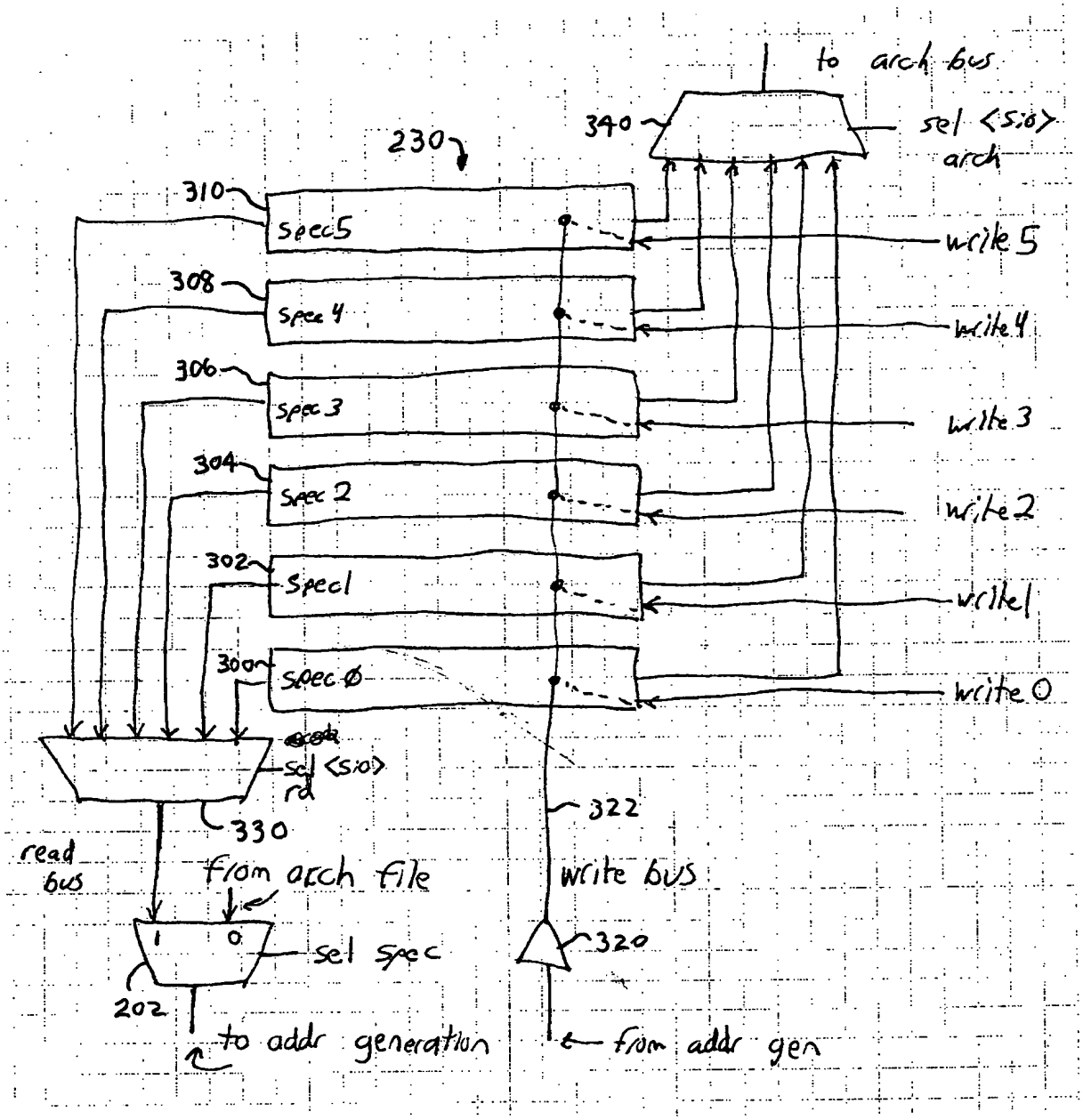
to arch bus
340
sel <5:0>
arch
230
310
spec5
write 5
308
spec 4
write 4
306
spec 3
write 3
304
spec 2
write 2
302
spec 1
write 1
300
spec Ø
write 0
sel <5:0>
rd
330
322
read bus
from arch file
write bus
1
0
sel spec
320
202
to addr generation
from addr gen

FIG. 4

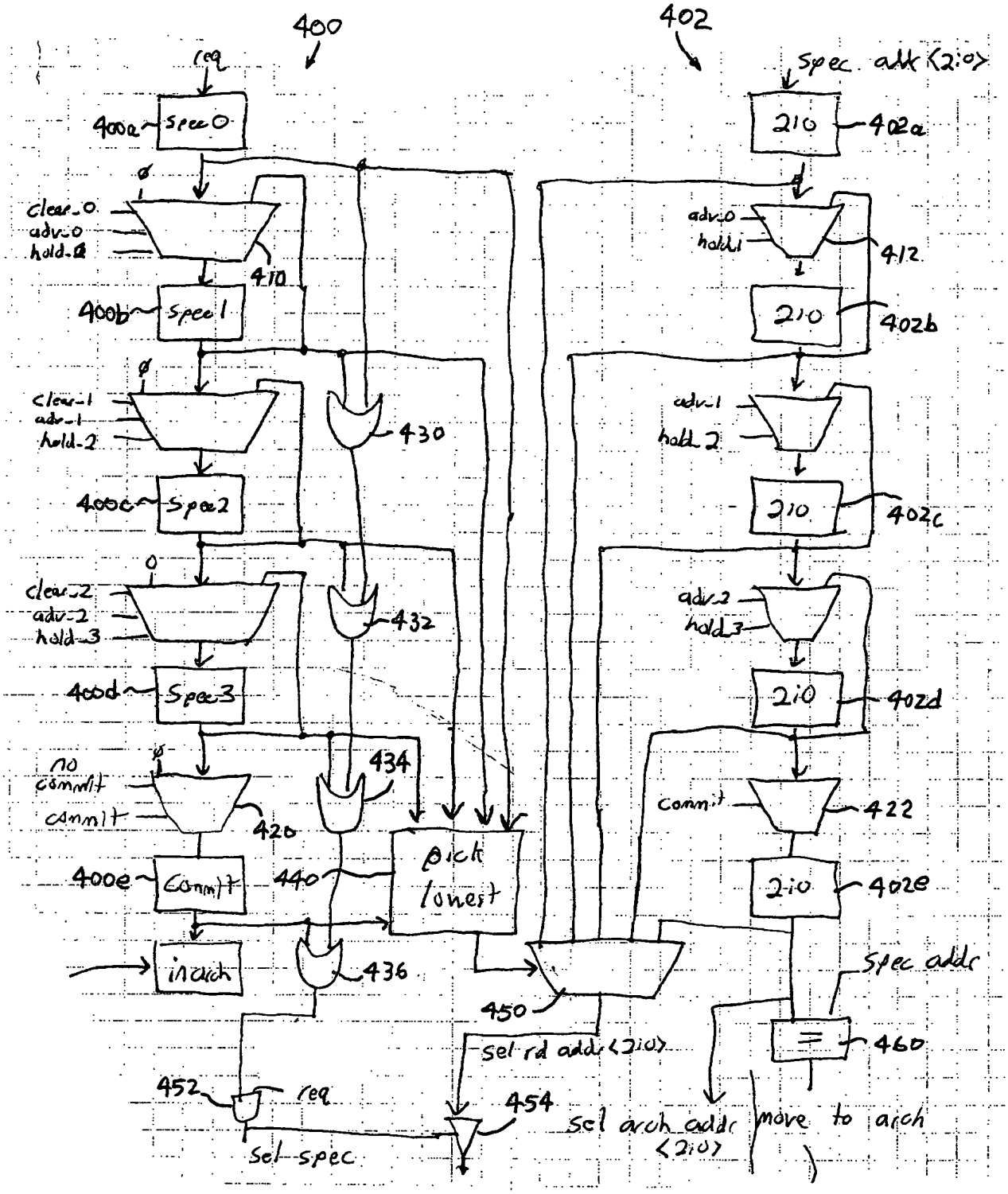
400
402
req
spec. addr <2:0>
400a
spec 0
210
402a
clear_0
adv_0
hold_0
410
adv_0
hold_1
412
400b
spec 1
210
402b
clear_1
adv_1
hold_2
430
adv_1
hold_2
400c
spec 2
210
402c
clear_2
adv_2
hold_3
432
adv_2
hold_3
400d
spec 3
210
402d
no commit
commit
420
434
commit
422
400e
commit
440
pick lowest
210
402e
in arch
436
spec addr
450
sel rd addr <2:0>
=
460
452
req
454
sel arch addr <2:0>
move to arch
sel spec

FIG. 5

Example 0

A r0 = [I0 ++ M0]

B r0 = [I0 ++ M0]

C r0 = [I0 ++ M0]

D r0 = [I0 ++ M0]

E r0 = [I0 ++ M0]

F r0 = [I0 ++ M0]

G r0 = [I0 ++ M0]

FIG. 6

INSTR A IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x0
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

400 402

SPEC RF

0	A
1	–
2	–
3	–
4	–
5	–

230

FIG. 7A

INSTR B IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x1
SPEC 1	1	0x0
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

400 402

SPEC RF

0	A
1	B
2	–
3	–
4	–
5	–

230

FIG. 7B

INSTR C IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x2
SPEC 1	1	0x1
SPEC 2	1	0x0
SPEC 3	0	0xX
COMMIT	0	0xX

400 402

SPEC RF

0	A
1	B
2	C
3	–
4	–
5	–

230

FIG. 7C

INSTR D IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x3
SPEC 1	1	0x2
SPEC 2	1	0x1
SPEC 3	1	0x0
COMMIT	0	0xX

400 402

SPEC RF

0	A
1	B
2	C
3	D
4	–
5	–

230

FIG. 7D

INSTR E IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x4
SPEC 1	1	0x3
SPEC 2	1	0x2
SPEC 3	1	0x1
COMMIT	1	0x0

400 402

SPEC RF

0	A
1	B
2	C
3	D
4	E
5	—

230

FIG. 7E

INSTR F IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x5
SPEC 1	1	0x4
SPEC 2	1	0x3
SPEC 3	1	0x2
COMMIT	1	0x1

SPEC RF

0	—
1	B
2	C
3	D
4	E
5	F

FIG. 7F

INSTR G IO

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x0
SPEC 1	1	0x5
SPEC 2	1	0x4
SPEC 3	1	0x3
COMMIT	1	0x2

SPEC RF

0	G
1	–
2	C
3	D
4	E
5	F

230

FIG. 7G

Example 1

A $r0 = [p0++]$

B $r1 = [p1++]$

C $r2 = [p1++]$

D $r3 = [p1++]$

E $r4 = [p1++]$

F $r5 = [p1++]$

G $r6 = [p1++]$

FIG. 8

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x0
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

C440 C442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xX
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

C450 C452

SPEC RF

0	A
1	–
2	–
3	–
4	–
5	–

C230

INSTR A

FIG. 9A

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xX
SPEC 1	1	0x0
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

C440 C442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x1
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

C450 C452

SPEC R.F

0	A
1	B
2	–
3	–
4	–
5	–

C230

INSTR B

FIG. 9B

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xx
SPEC 1	0	0xX
SPEC 2	1	0x0
SPEC 3	0	0xX
COMMIT	0	0xX

440 442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x2
SPEC 1	1	0x1
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

450 452

SPEC RF

0	A
1	B
2	C
3	—
4	—
5	—

230

INSTR C

FIG. 9C

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xX
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	1	0x0
COMMIT	0	0xX

440 442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x3
SPEC 1	1	0x2
SPEC 2	1	0x1
SPEC 3	0	0xX
COMMIT	0	0xX

450 452

SPEC RF

0	A
1	B
2	C
3	D
4	
5	

230

INSTR D

FIG. 9D

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xX
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	1	0x0

C440 C442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x4
SPEC 1	1	0x3
SPEC 2	1	0x2
SPEC 3	1	0x1
COMMIT	0	0xX

C450 C452

SPEC RF

0	A
1	B
2	C
3	D
4	E
5	—

C230

INSTR E

FIG. 9E

P0

STAGE	IN SPEC REG	ADDR REG
SPEC 0	0	0xX
SPEC 1	0	0xX
SPEC 2	0	0xX
SPEC 3	0	0xX
COMMIT	0	0xX

440 442

P1

STAGE	IN SPEC REG	ADDR REG
SPEC 0	1	0x5
SPEC 1	1	0x4
SPEC 2	1	0x3
SPEC 3	1	0x2
COMMIT	1	0x1

450 452

SPEC RF

0	—
1	B
2	C
3	D
4	E
5	F

230

INSTR F

FIG. 9F